

# M5L 2716 K, K-65

## 16 384-BIT (2048-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### DESCRIPTION

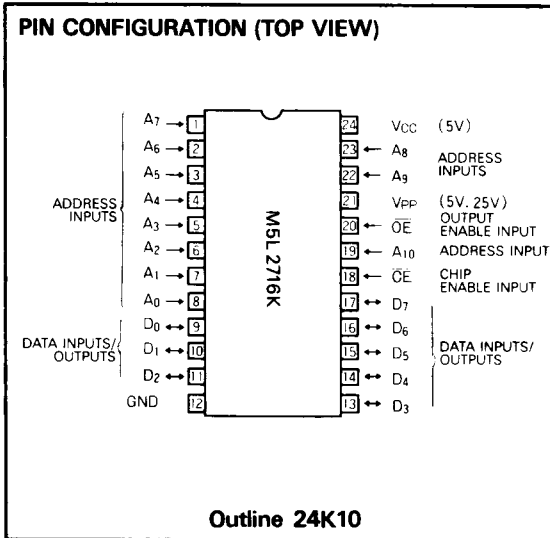
These are ultraviolet-light erasable and electrically reprogrammable 16 384-bit (2048-word by 8-bit) EPROMs. They incorporate N-channel silicon-gate MOS technology, and are designed for microprocessor programming applications.

### FEATURES

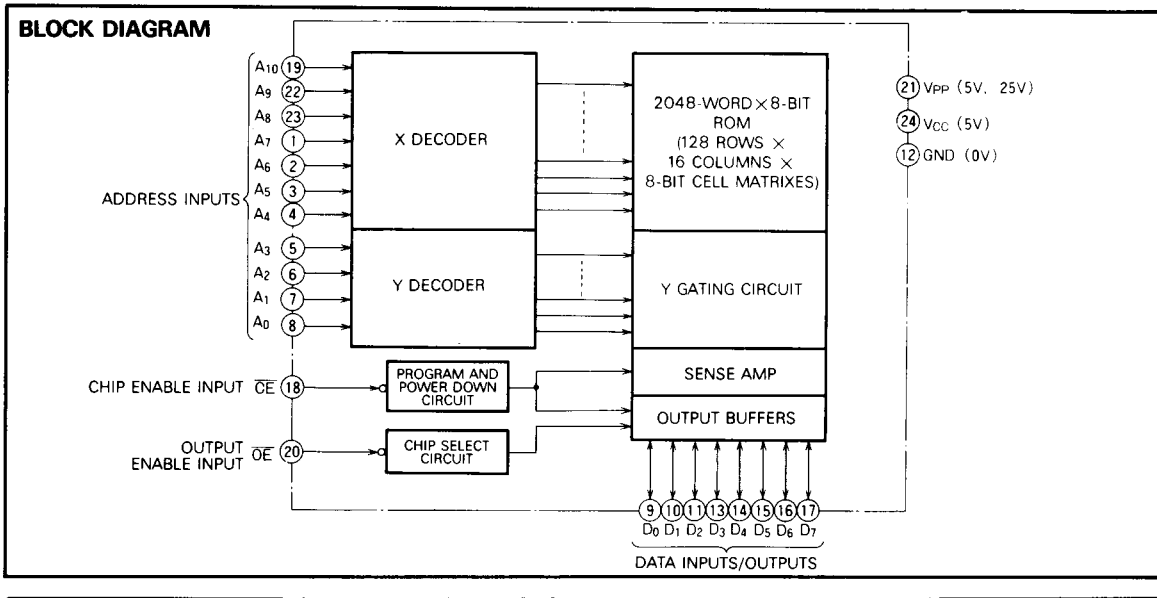
- Fast programming : 100s/16 384 bits (typ)
- Access time M5L 2716K : 450ns (max)  
M5L 2716K-65 : 650ns (max)
- Static circuits are used throughout
- Inputs and outputs TTL-compatible in read and program modes
- Single 5V power supply for read mode  
(25V power supply required for program)
- Low power dissipation: Operating : 525mW (max)  
Standby : 132mW (max)
- Single-location programming  
(requires one 50ms pulse/address)
- Interchangeable with Intel's 2716 in pin configuration and electrical characteristics

### APPLICATION

- Computers and peripheral equipment



5



# M5L 2716 K, K-65

## 16 384-BIT (2048-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### FUNCTION

#### Read

Set the  $\overline{CE}$  and  $\overline{OE}$  terminals to the read mode (low-level). Low-level input to  $\overline{CE}$  and  $\overline{OE}$  and address signals to the address inputs ( $A_0 \sim A_{10}$ ) make the data contents of the designated address location available at the data inputs/outputs ( $D_0 \sim D_7$ ). When the  $\overline{CE}$  or  $\overline{OE}$  signal is high, data inputs/outputs ( $D_0 \sim D_7$ ) are in a floating state.

When the  $\overline{CE}$  signal is high, the device is in the standby mode or power-down mode.

#### Programming

The chip enters the programming mode when 25V is supplied to the  $V_{PP}$  power supply input and  $\overline{OE}$  is at high-level. A location is designated by address signals  $A_0 \sim A_{10}$ , and the data to be programmed must be applied at 8 bits in parallel to the data inputs  $D_0 \sim D_7$ . A program pulse to the  $\overline{CE}$  at this state will effect programming. Only one programming pulse is required, but its width must satisfy the condition  $45ms \leq t_{w(CE)} \leq 55ms$ .

#### Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15Ws/cm<sup>2</sup>.

#### Mode selection

(Unit: V)

Mode	P <sub>in</sub>	$\overline{CE}$	$\overline{OE}$	$V_{PP}$	$V_{CC}$	
Read		$V_{IL}$	$V_{IL}$	5	5	Output
Deselect		$V_{IL} \sim V_{IH}$	$V_{IH}$	5	5	Floating
Power down		$V_{IH}$	$V_{IL} \sim V_{IH}$	5	5	Floating
Program		Pulsed $V_{IL}$ to $V_{IH}$	$V_{IH}$	25	5	Input
Program verify		$V_{IL}$	$V_{IL}$	5 or 25	5	Output
Program inhibit		$V_{IL}$	$V_{IH}$	25	5	Floating

### PRECAUTIONS FOR READ OPERATION

- $V_{CC}$  should be turned on with or before  $V_{PP}$  and turned off with or after  $V_{PP}$ .
- $V_{PP}$  should be connected directly to  $V_{CC}$  except during programming. For supply current design, therefore,  $V_{PP}$  and  $V_{CC}$  should be added.

### HANDLING PRECAUTIONS

- Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent window should be covered with opaque tape.
- High voltages are used when programming, and the conditions under which it is performed must be carefully controlled to prevent the application of excessively high voltages. Specifically, the voltage applied to  $V_{PP}$  should be kept below 26V including overshoot. Special precautions should be taken at the time of power-on.
- Before erasing, clean the surface of the transparent lid to remove completely oily impurities or paste, which may impede irradiation and affect the erasing characteristics.

# M5L 2716 K, K-65

## 16 384-BIT (2048-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Limits	Unit
V <sub>I1</sub>	Input voltage, V <sub>pp</sub>	With respect to GND	-0.3 - 26.5	V
V <sub>I2</sub>	Input voltage, V <sub>CC</sub> , address, $\overline{OE}$ , $\overline{CE}$ , data		-0.3 - 6	V
T <sub>opr</sub>	Operating free-air temperature range		0 - 70	°C
T <sub>stg</sub>	Storage temperature range		-65 - 125	°C

### READ OPERATION

**Recommended Operating Conditions** (T<sub>a</sub> = 0 - 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
V <sub>PP</sub>	Supply voltage	(V <sub>PP</sub> = V <sub>CC</sub> )			V
GND	Supply voltage		0		V
V <sub>IL</sub>	Low-level input voltage	-0.1		0.8	V
V <sub>IH</sub>	High-level input voltage	2.2		V <sub>CC</sub> + 1	V

**Electrical Characteristics** (T<sub>a</sub> = 0 - 70°C, V<sub>CC</sub> = 5 V ± 5%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)

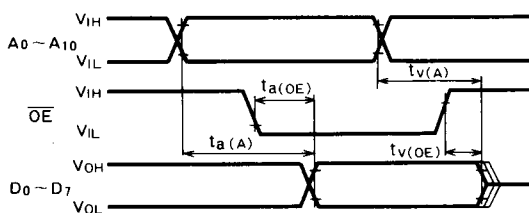
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ (Note 1)	Max	
I <sub>IL</sub>	High-level input current, address, $\overline{OE}$ , $\overline{CE}$	V <sub>I</sub> = 5.25V			10	μA
I <sub>OZ</sub>	Off-state output current	V <sub>O</sub> = 5.25V, $\overline{OE}$ = 5 V			10	μA
I <sub>PP1</sub>	Supply current from V <sub>PP</sub>	V <sub>PP</sub> = 5.85V			6	mA
I <sub>CC1</sub>	Supply current from V <sub>CC</sub> (standby)	$\overline{OE}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IL</sub>		10	25	mA
I <sub>CC2</sub>	Supply current from V <sub>CC</sub> (operating)	$\overline{OE}$ = $\overline{CE}$ = V <sub>IL</sub>		57	100	mA
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -400μA	2.4			V

**Switching Characteristics** (T<sub>a</sub> = 0 - 70°C, V<sub>CC</sub> = 5 V ± 5%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)

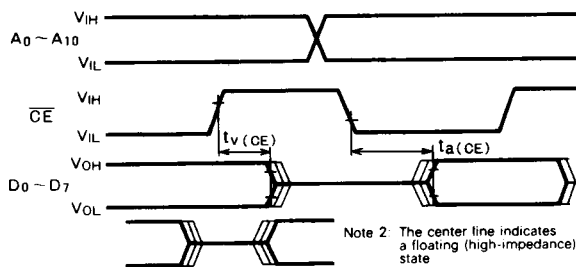
Symbol	Parameter	Test conditions	Limits			Unit		
			Min	Typ (Note 1)	Max			
t <sub>a(A)</sub>	Address access time	M5L 2716K	$\overline{OE} = \overline{CE} = V_{IL}$	t <sub>r</sub> ≤ 20ns		450	ns	
		M5L 2716K - 65				t <sub>f</sub> ≤ 20ns	650	ns
t <sub>a(OE)</sub>	Chip enable access time	M5L 2716K	$\overline{OE} = V_{IL}$	V <sub>IL</sub> = 0.8V	V <sub>IH</sub> = 2.2V	450	ns	
		M5L 2716K - 65				650	ns	
t <sub>a(OE)</sub>	Output enable access time	M5L 2716K	$\overline{OE} = V_{IL}$			80	150	ns
		M5L 2716K - 65				300	ns	
t <sub>v(OE)</sub>	Data valid time after output enable	$\overline{OE} = V_{IL}$				0	100	ns
t <sub>v(OE)</sub>	Data valid time after chip select	$\overline{CE} = V_{IL}$				0	100	ns
t <sub>v(A)</sub>	Data valid time after address	$\overline{OE} = \overline{CE} = V_{IL}$				0		ns

Note 1: at T<sub>a</sub> = 25°C and normal supply voltage.

### Timing Diagrams (Read Operation) When Power-Down Mode Not Used



### Power-Down Mode



# M5L 2716 K, K-65

## 16 384-BIT (2048-WORD BY 8-BIT)

### ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

#### PROGRAM MODE

**Recommended Operating Conditions** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{PP}$	Supply voltage	24	25	26	V
GNG	Supply voltage		0		V
$V_{IL}$	Low-level input voltage	-0.1		0.8	V
$V_{IH}$	High-level input voltage	2.2		$V_{CC} + 1$	V

**Electrical Characteristics** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V} \pm 5 \%$ ,  $V_{PP} = 25 \pm 1 \text{ V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{IL}$	High-level input current, address: $\overline{OE}$ , $\overline{CE}$	$V_{IN} = 5.25 \text{ V}$			10	$\mu\text{A}$
$I_{PP1}$	Supply current from $V_{PP}$	$\overline{CE} = V_{IL}$			6	mA
$I_{PP2}$	Supply current from $V_{PP}$	$\overline{CE} = V_{IH}$			30	mA
$I_{CC}$	Supply current from $V_{CC}$				100	mA

**Timing Requirements** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V} \pm 5 \%$ ,  $V_{PP} = 25 \pm 1 \text{ V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su}(A-CE)$	Address setup time before chip enable		2			$\mu\text{s}$
$t_{su}(OE-CE)$	Output enable setup time before chip enable		2			$\mu\text{s}$
$t_{su}(DQ-CE)$	Data input setup time before chip enable		2			$\mu\text{s}$
$t_h(CE-A)$	Address hold time after chip enable		2			$\mu\text{s}$
$t_h(CE-OE)$	Output enable hold time after chip enable		2			$\mu\text{s}$
$t_h(CE-DQ)$	Data input hold time after chip enable		2			$\mu\text{s}$
$t_w(CE)$	Chip enable pulse width		45	50	55	ms
$t_r(CE)$	Chip enable pulse rise time		5			ns
$t_f(CE)$	Chip enable pulse fall time		5			ns

**Switching Characteristics** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{CC} = 5 \text{ V} \pm 5 \%$ ,  $V_{PP} = 25 \pm 1 \text{ V}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_v(OE)$	Data valid time after output enable		0		120	ns
$t_a(OE)$	Output enable access time	M5L 2716K			150	ns
		M5L 2716K-65			300	ns

#### Timing Diagram (for Program and Verify)

