

4496203 HITACHI/ LOGIC/ARRAYS/MEM

04E 13082 D

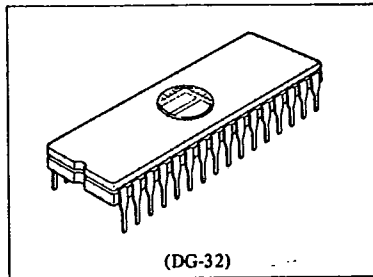
# HN27C101G Series

T-46-13-29

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply ..... +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode ..... Program Voltage: +12.5V DC ..... High Performance Programming Available
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time ..... 170/200/250ns (max.)
- Low power Dissipation ... 50mW/MHz typ. (Active Mode) 5μW typ. (Standby Mode)
- Pin Arrangement ..... 32 Pin JEDEC Standard

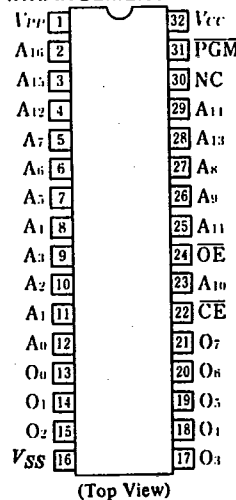


(DG-32)

■ ORDERING INFORMATION

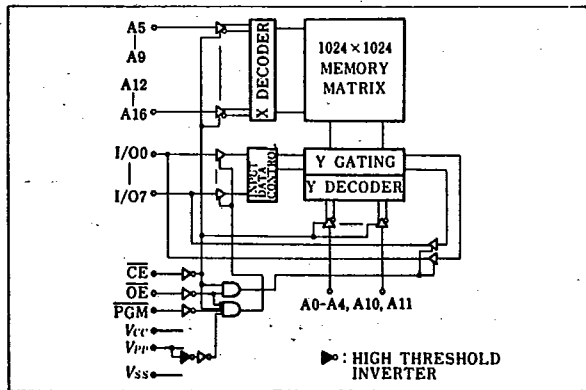
| Type No.     | Access Time | Package               |
|--------------|-------------|-----------------------|
| HN27C101G-17 | 170ns       | 600 mil 32 pin Cerdip |
| HN27C101G-20 | 200ns       |                       |
| HN27C101G-25 | 250ns       |                       |

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

| Mode            | Pins | CE (22)         | OE (24)         | PGM (31)        | V <sub>PP</sub> (1) | V <sub>CC</sub> (32) | Outputs (13~15, 17~21) |
|-----------------|------|-----------------|-----------------|-----------------|---------------------|----------------------|------------------------|
| Read            |      | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>CC</sub>     | V <sub>CC</sub>      | Dout                   |
| Output Disable  |      | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>CC</sub>     | V <sub>CC</sub>      | High Z                 |
| Standby         |      | V <sub>IH</sub> | X               | X               | V <sub>CC</sub>     | V <sub>CC</sub>      | High Z                 |
| Program         |      | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | Din                    |
| Program Verify  |      | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | Dout                   |
| Page Data Latch |      | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | Din                    |
| Page Program    |      | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | High Z                 |
| Program Inhibit |      | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>PP</sub>     | V <sub>CC</sub>      | High Z                 |
|                 |      | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub> |                     |                      |                        |
|                 |      | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>IL</sub> |                     |                      |                        |
|                 |      | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub> |                     |                      |                        |

Notes) 1. X: Don't care  
2. 30 pin should be connected to 32 pin.



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■ ABSOLUTE MAXIMUM RATINGS

| Item                                 | Symbol            | Value          | Unit |
|--------------------------------------|-------------------|----------------|------|
| All Input and Output Voltage*1       | $V_{in}, V_{out}$ | -0.6*2 to +7.0 | V    |
| $V_{PP}$ Voltage*1                   | $V_{PP}$          | -0.6 to +13.0  | V    |
| $V_{CC}$ Voltage*1                   | $V_{CC}$          | -0.6 to +7.0   | V    |
| Operating Temperature Range          | $T_{opr}$         | 0 to +70       | °C   |
| Storage Temperature Range            | $T_{stg}$         | -65 to +125    | °C   |
| Storage Temperature Range Under Bias | $T_{bias}$        | -10 to +80     | °C   |

Notes) \*1. With respect to  $V_{SS}$   
 \*2. -1.0V for pulse width  $\leq$  50ns.

■ READ OPERATION

● DC CHARACTERISTICS ( $T_a = 0$  to +70°C,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = V_{CC}$ )

| Parameter              | Symbol    | Test Conditions                         | min.   | typ. | max.            | Unit    |
|------------------------|-----------|---|--------|------|-----------------|---------|
| Input Leakage Current  | $I_{LI}$  | $V_{in} = 5.25V$                        | -      | -    | 2               | $\mu A$ |
| Output Leakage Current | $I_{LO}$  | $V_{out} = 5.25V/0.45V$                 | -      | -    | 2               | $\mu A$ |
| $V_{PP}$ Current       | $I_{PP1}$ | $V_{PP} = 5.5V$                         | -      | 1    | 20              | $\mu A$ |
| $V_{CC}$ Current       | $I_{SB1}$ | $\overline{CE} = V_{IH}$                | -      | -    | 1               | mA      |
|                        | $I_{SB2}$ | $\overline{CE} = V_{CC} \pm 0.3V$       | -      | 1    | 20              | $\mu A$ |
| $V_{CC}$ Current       | $I_{CC1}$ | $\overline{CE} = V_{IL}, I_{out} = 0mA$ | -      | -    | 30              | mA      |
|                        | $I_{CC2}$ | $f = 5MHz, I_{out} = 0mA$               | -      | -    | 30              | mA      |
|                        | $I_{CC3}$ | $f = 1MHz, I_{out} = 0mA$               | -      | -    | 15              | mA      |
| Input Low Voltage      | $V_{IL}$  |   | -0.3*1 | -    | 0.8             | V       |
| Input High Voltage     | $V_{IH}$  |   | 2.2    | -    | $V_{CC} + 1$ *2 | V       |
| Output Low Voltage     | $V_{OL}$  | $I_{OL} = 2.1mA$                        | -      | -    | 0.45            | V       |
| Output High Voltage    | $V_{OH}$  | $I_{OH} = -400\mu A$                    | 2.4    | -    | -               | V       |

Notes) \*1. -1.0V for pulse width  $\leq$  50ns.  
 \*2.  $V_{CC} + 1.5V$  for pulse width  $\leq$  20ns. If  $V_{IH}$  is over the specified maximum value, read operation cannot be guaranteed.

● AC CHARACTERISTICS ( $T_a = 0$  to +70°C,  $V_{CC} = 5V \pm 5\%$ ,  $V_{PP} = V_{CC}$ )

| Parameter                            | Symbol    | Test Conditions                          | HN27C101G-17 |      | HN27C101G-20 |      | HN27C101G-25 |      | Unit |
|--------------------------------------|-----------|--|--------------|------|--------------|------|--------------|------|------|
|                                      |           |  | min.         | max. | min.         | max. | min.         | max. |      |
| Address to Output Delay              | $t_{ACC}$ | $\overline{CE} = \overline{OE} = V_{IL}$ | -            | 170  | -            | 200  | -            | 250  | ns   |
| $\overline{CE}$ to Output Delay      | $t_{CE}$  | $\overline{OE} = V_{IL}$                 | -            | 170  | -            | 200  | -            | 250  | ns   |
| $\overline{OE}$ to Output Delay      | $t_{OE}$  | $\overline{CE} = V_{IL}$                 | 10           | 70   | 10           | 70   | 10           | 100  | ns   |
| $\overline{OE}$ High to Output Float | $t_{DF}$  | $\overline{CE} = V_{IL}$                 | 0            | 50   | 0            | 50   | 0            | 60   | ns   |
| Address to Output Hold               | $t_{OH}$  | $\overline{CE} = \overline{OE} = V_{IL}$ | 0            | -    | 0            | -    | 0            | -    | ns   |

Note)  $t_{DF}$  defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

● Test Condition Input Pulse Levels: 0.45V to 2.4V  
 Input Rise and Fall Time:  $\leq$  20ns  
 Output Load: 1 TTL Gate + 100pF  
 Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V  
 Outputs; 0.8V and 2.0V

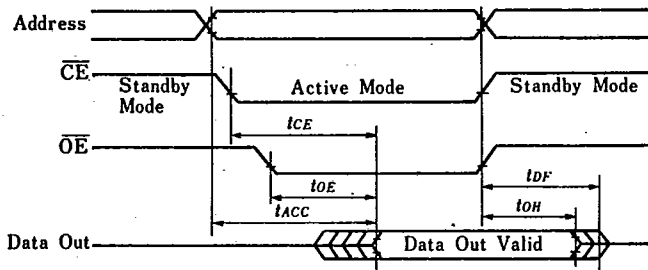


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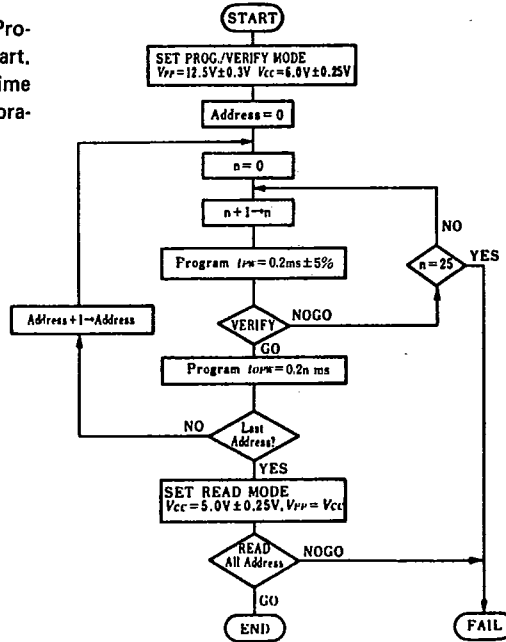


● CAPACITANCE ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

| Parameter          | Symbol    | Test Conditions       | min. | typ. | max. | Unit |
|--------------------|-----------|-----------------------|------|------|------|------|
| Input Capacitance  | $C_{in}$  | $V_{in} = 0\text{V}$  | -    | -    | 10   | pF   |
| Output Capacitance | $C_{out}$ | $V_{out} = 0\text{V}$ | -    | -    | 15   | pF   |

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart



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• DC PROGRAMMING CHARACTERISTICS ( $T_a=25^\circ\text{C}\pm 5^\circ\text{C}$ ,  $V_{CC}=6\text{V}\pm 0.25\text{V}$ ,  $V_{PP}=12.5\text{V}\pm 0.3\text{V}$ )

| Parameter                         | Symbol   | Test Conditions                              | min.               | typ. | max.                       | Unit          |
|-----------------------------------|----------|--|--------------------|------|----------------------------|---------------|
| Input Leakage Current             | $I_{LI}$ | $V_{in}=6.25\text{V}/0.45\text{V}$           | -                  | -    | 2                          | $\mu\text{A}$ |
| Output Low Voltage during Verify  | $V_{OL}$ | $I_{OL}=2.1\text{mA}$                        | -                  | -    | 0.45                       | V             |
| Output High Voltage during Verify | $V_{OH}$ | $I_{OH}=-400\mu\text{A}$                     | 2.4                | -    | -                          | V             |
| $V_{CC}$ Current (Active)         | $I_{CC}$ |  | -                  | -    | 30                         | mA            |
| Input Low Level                   | $V_{IL}$ |  | -0.1 <sup>*5</sup> | -    | 0.8                        | V             |
| Input High Level                  | $V_{IH}$ |  | 2.2                | -    | $V_{CC}+0.5$ <sup>*6</sup> | V             |
| $V_{PP}$ Supply Current           | $I_{PP}$ | $\overline{\text{CE}} = \text{PGM} = V_{IL}$ | -                  | -    | 40                         | mA            |

- Notes) \*1.  $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .  
 \*2.  $V_{PP}$  must not exceed 13V including overshoot.  
 \*3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP}=12.5\text{V}$ .  
 \*4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5V or 12.5V to  $V_{IL}$  when  $\overline{\text{CE}} = \text{Low}$ .  
 \*5. -0.6V for pulse width  $\leq 20\text{ns}$ .  
 \*6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

( $T_a=25^\circ\text{C}\pm 5^\circ\text{C}$ ,  $V_{CC}=6\text{V}\pm 0.25\text{V}$ ,  $V_{PP}=12.5\text{V}\pm 0.3\text{V}$ )

| Parameter                                    | Symbol                  | Test Conditions | min. | typ. | max. | Unit          |
|--|-------------------------|-----------------|------|------|------|---------------|
| Address Setup Time                           | $t_{AS}$                |                 | 2    | -    | -    | $\mu\text{s}$ |
| $\overline{\text{OE}}$ Setup Time            | $t_{OES}$               |                 | 2    | -    | -    | $\mu\text{s}$ |
| Data Setup Time                              | $t_{DS}$                |                 | 2    | -    | -    | $\mu\text{s}$ |
| Address Hold Time                            | $t_{AH}$                |                 | 0    | -    | -    | $\mu\text{s}$ |
| Data Hold Time                               | $t_{DH}$                |                 | 2    | -    | -    | $\mu\text{s}$ |
| $\overline{\text{OE}}$ to Output Float Delay | $t_{DF}$ <sup>*1</sup>  |                 | 0    | -    | 130  | ns            |
| $V_{PP}$ Setup Time                          | $t_{VPS}$               |                 | 2    | -    | -    | $\mu\text{s}$ |
| $V_{CC}$ Setup Time                          | $t_{VCS}$               |                 | 2    | -    | -    | $\mu\text{s}$ |
| PGM Pulse Width during Initial Programming   | $t_{PW}$                |                 | 0.19 | 0.2  | 0.21 | ms            |
| PGM Pulse Width during Overprogramming       | $t_{OPW}$ <sup>*2</sup> |                 | 0.19 | -    | 5.25 | ms            |
| $\overline{\text{CE}}$ Setup Time            | $t_{CES}$               |                 | 2    | -    | -    | $\mu\text{s}$ |
| Data Valid from $\overline{\text{OE}}$       | $t_{OE}$                |                 | 0    | -    | 150  | ns            |

- Notes) \*1.  $t_{DF}$  defines the time at which the output achieves the open circuit condition and data is no longer driven.  
 \*2.  $t_{OPW}$  is defined as mentioned in flowchart.



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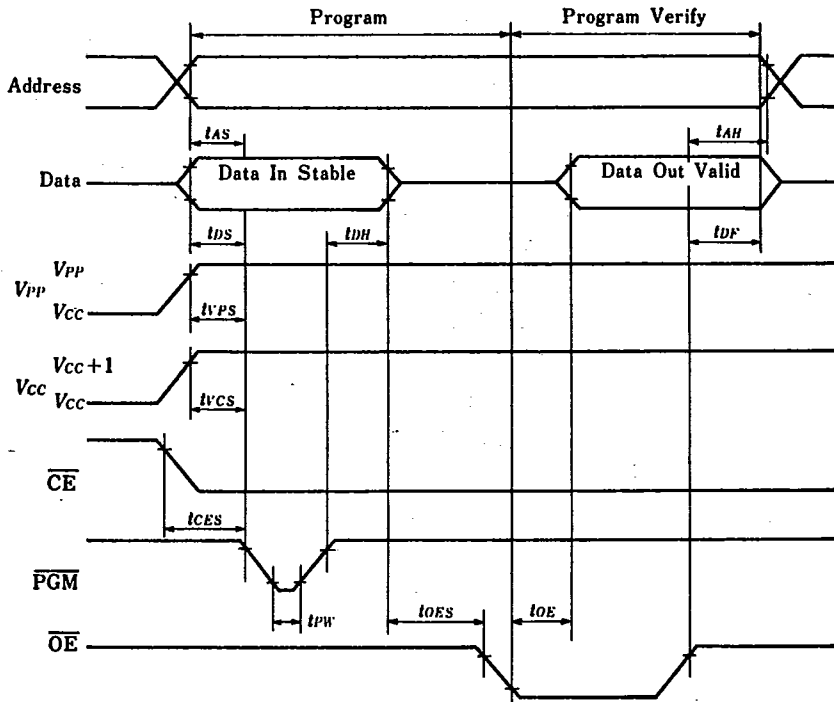
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● SWITCHING CHARACTERISTICS

Input Pulse Levels: 0.45V to 2.4V  
 Input Rise and Fall Time:  $\leq 20\text{ns}$   
 Reference Levels for Measurement: Inputs; 0.8V and 2.0V  
 Timing: Outputs; 0.8V and 2.0V



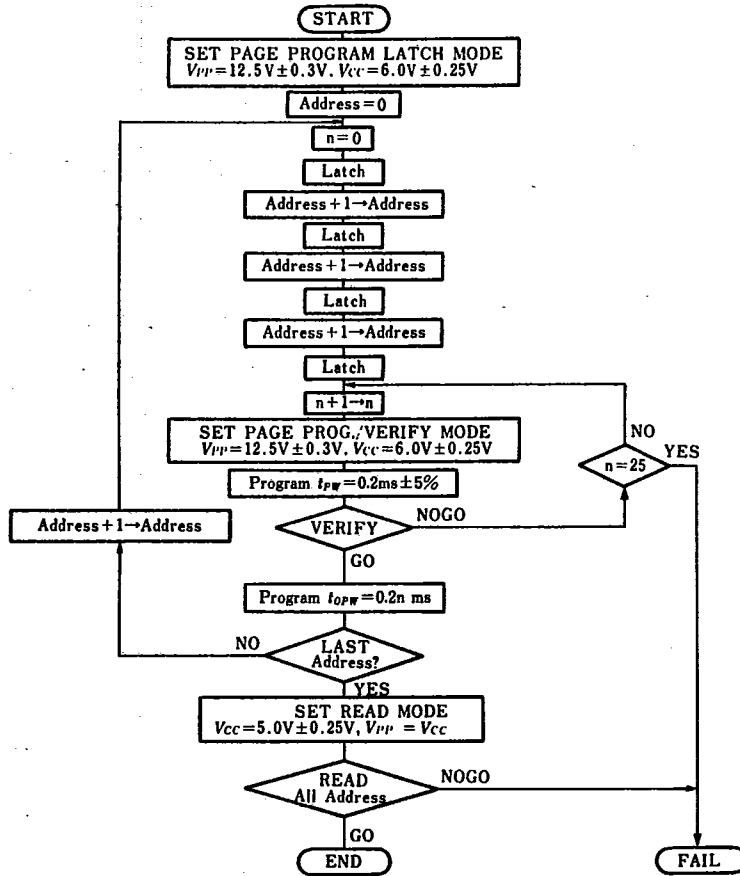
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■ HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS (T<sub>a</sub>=25°C ±5°C, V<sub>CC</sub>=6V ±0.25V, V<sub>PP</sub>=12.5V ±0.3V)

| Parameter                         | Symbol          | Test Conditions                             | min.               | typ. | max.                               | Unit |
|-----------------------------------|-----------------|---|--------------------|------|------------------------------------|------|
| Input Leakage Current             | I <sub>LI</sub> | V <sub>In</sub> = 6.25V/0.45V               | -                  | -    | 2                                  | μA   |
| Output Low Voltage during Verify  | V <sub>OL</sub> | I <sub>OL</sub> = 2.1mA                     | -                  | -    | 0.45                               | V    |
| Output High Voltage during Verify | V <sub>OH</sub> | I <sub>OH</sub> = -400μA                    | 2.4                | -    | -                                  | V    |
| V <sub>CC</sub> Current (Active)  | I <sub>CC</sub> |   | -                  | -    | 30                                 | mA   |
| Input Low Level                   | V <sub>IL</sub> |   | -0.1 <sup>*5</sup> | -    | 0.8                                | V    |
| Input High Level                  | V <sub>IH</sub> |   | 2.2                | -    | V <sub>CC</sub> +0.5 <sup>*6</sup> | V    |
| V <sub>PP</sub> Supply Current    | I <sub>PP</sub> | CE=OE=V <sub>IH</sub> , PGM=V <sub>IL</sub> | -                  | -    | 50                                 | mA   |

- Notes) \*1. V<sub>CC</sub> must be applied before V<sub>PP</sub> and removed after V<sub>PP</sub>.  
 \*2. V<sub>PP</sub> must not exceed 13V including overshoot.  
 \*3. An influence may be had upon device reliability if the device is installed or removed while V<sub>PP</sub>=12.5V.  
 \*4. Do not alter V<sub>PP</sub> either V<sub>IL</sub> to 12.5V or 12.5V to V<sub>IL</sub> when CE=Low.  
 \*5. -0.6V for pulse width ≤ 20ns  
 \*6. If V<sub>IH</sub> is over the specified maximum value, programming operation cannot be guaranteed.



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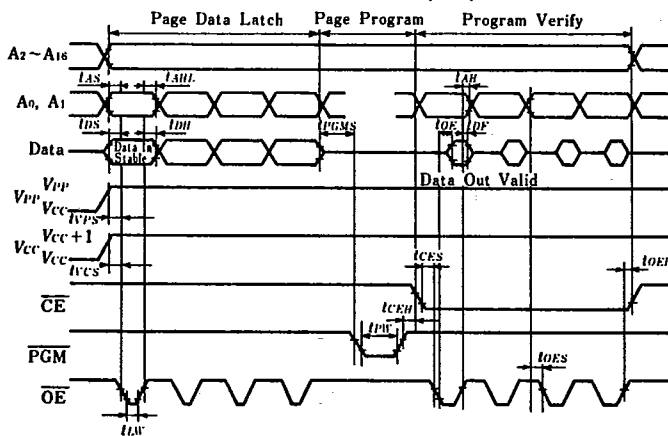
● AC PROGRAMMING CHARACTERISTICS  
 ( $T_a=25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC}=6\text{V} \pm 0.25\text{V}$ ,  $V_{PP}=12.5\text{V} \pm 0.3\text{V}$ )

| Parameter                                  | Symbol         | Test Conditions | min. | typ. | max. | Unit          |
|--|----------------|-----------------|------|------|------|---------------|
| Address Setup Time                         | $t_{AS}$       |                 | 2    | -    | -    | $\mu\text{s}$ |
| OE Setup Time                              | $t_{OES}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| Data Setup Time                            | $t_{DS}$       |                 | 2    | -    | -    | $\mu\text{s}$ |
| Address Hold Time                          | $t_{AH}$       |                 | 0    | -    | -    | $\mu\text{s}$ |
|  | $t_{AHL}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| Data Hold Time                             | $t_{DH}$       |                 | 2    | -    | -    | $\mu\text{s}$ |
| OE to Output Float Delay                   | $t_{DF}^{*1}$  |                 | 0    | -    | 130  | ns            |
| $V_{PP}$ Setup Time                        | $t_{VPS}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| $V_{CC}$ Setup Time                        | $t_{VCS}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| PGM Pulse Width during Initial Programming | $t_{PW}$       |                 | 0.19 | 0.2  | 0.21 | ms            |
| PGM Pulse Width during Overprogramming     | $t_{OPW}^{*2}$ |                 | 0.19 | -    | 5.25 | ms            |
| CE Setup Time                              | $t_{CES}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| Data Valid from OE                         | $t_{OE}$       |                 | 0    | -    | 150  | ns            |
| OE Pulse Width during Data Latch           | $t_{LW}$       |                 | 1    | -    | -    | $\mu\text{s}$ |
| PGM Setup Time                             | $t_{PGMS}$     |                 | 2    | -    | -    | $\mu\text{s}$ |
| CE Hold Time                               | $t_{CEH}$      |                 | 2    | -    | -    | $\mu\text{s}$ |
| OE Hold Time                               | $t_{OEH}$      |                 | 2    | -    | -    | $\mu\text{s}$ |

Notes) \*1.  $t_{DF}$  defines the time at which the output achieves the open circuit condition and data is no longer driven.  
 \*2.  $t_{OPW}$  is defined as mentioned in flowchart.

● SWITCHING CHARACTERISTICS

- Test Condition Input Pulse Levels: 0.45V to 2.4V
- Input Rise and Fall Time:  $\leq 20\text{ns}$
- Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
- Outputs; 0.8V and 2.0V



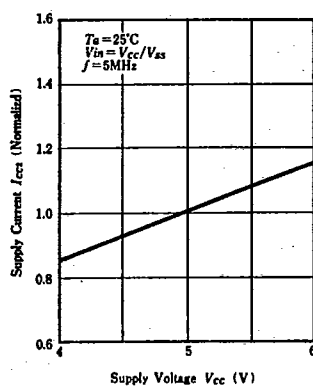
■ ERASE

Erase of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W·sec/cm<sup>2</sup>

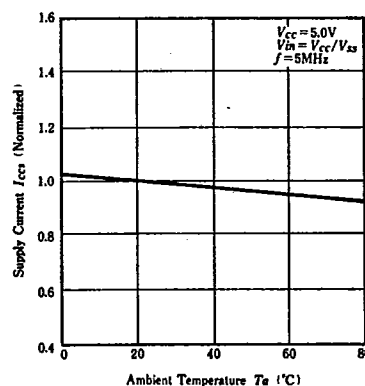


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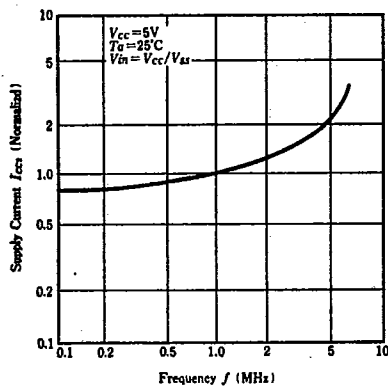
SUPPLY CURRENT vs. SUPPLY VOLTAGE



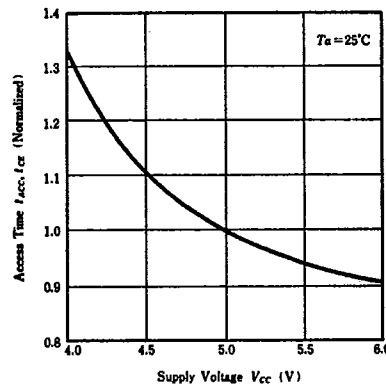
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE

