

## 2K (256 x 8) UV ERASABLE PROM

1702A-2	0.65 us Max.
1702A	1.0 us Max.
1702A-6	1.5 us Max.

- **Fast Access Time: Max. 650 ns (1702A-2)**
  - **Fast Programming: 2 Minutes for all 2048 Bits**
  - **All 2048 Bits Guaranteed\* Programmable: 100% Factory Tested**
- **Static MOS: No Clocks Required**
  - **Inputs and Outputs DTL and TTL Compatible**
  - **Three-State Output: OR-tie Capability**

PROM/ROM

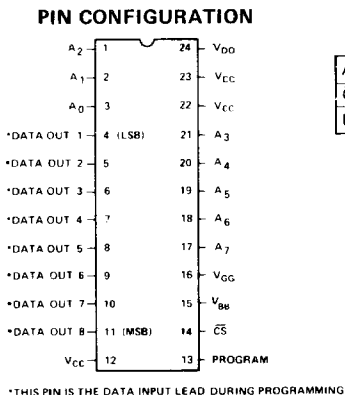
The 1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The 1702A undergoes complete programming and functional testing prior to shipment, thus insuring 100% programmability.

Initially all 2048 bits of the 1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit location. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the 1702A to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The circuitry of the 1702A is completely static. No clocks are required. Access times from 650ns to 1.5µs are available. A 1702AL family is available (see 1702AL data sheets for specifications) for those systems requiring lower power dissipation than the 1702A.

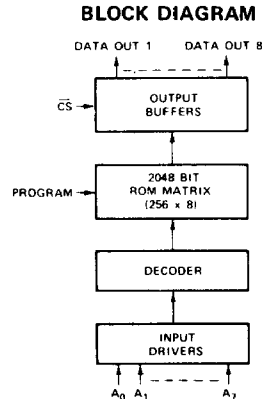
The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

\*Intel's liability shall be limited to replacing any unit which fails to program as desired.



### PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT1} - D_{OUT8}$	Data Outputs



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

## PIN CONNECTIONS

The external lead connections to the 1702A differ, depending on whether the device is being programmed or used in read mode (see following table). In the programming mode, the data inputs 1-8 are pins 4-11 respectively. *The programming voltages and timing are shown in the Data Catalog ROM and PROM Programming Instructions section.*

MODE \ PIN	12 (V <sub>CC</sub> )	13 (Program)	14 ( $\overline{CS}$ )	15 (V <sub>BB</sub> )	16 (V <sub>GG</sub> )	22 (V <sub>CC</sub> )	23 (V <sub>CC</sub> )	24 (V <sub>DD</sub> )
Read	V <sub>CC</sub>	V <sub>CC</sub>	GND	V <sub>CC</sub>	V <sub>GG</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>DD</sub>
Programming	GND	Program Pulse	GND	V <sub>BB</sub>	Pulsed V <sub>GG</sub>	GND	GND	Pulsed V <sub>DD</sub>

## Absolute Maximum Ratings\*

Ambient Temperature Under Bias . . . . . -10°C to +80°C  
 Storage Temperature . . . . . -65°C to +125°C  
 Soldering Temperature of Leads (10 sec) . . . . . +300°C  
 Power Dissipation . . . . . 2 Watts  
 Read Operation: Input Voltages and Supply  
   Voltages with respect to V<sub>CC</sub> . . . . . +0.5V to -20V  
 Program Operation: Input Voltages and Supply  
   Voltages with respect to V<sub>CC</sub> . . . . . -48V

### \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## D.C. and Operating Characteristics

T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = +5V ±5%, V<sub>DD</sub> = -9V ±5%, V<sub>GG</sub> = -9V ±5%, unless otherwise noted.

### READ OPERATION

Symbol	Test	1702A, 1702A-6 Limits			1702A-2 Limits			Unit	Conditions
		Min.	Typ. <sup>[1]</sup>	Max.	Min.	Typ. <sup>[1]</sup>	Max.		
I <sub>LI</sub>	Address and Chip Select Input Load Current			1			1	μA	V <sub>IN</sub> = 0.0V
I <sub>LO</sub>	Output Leakage Current			1			1	μA	V <sub>OUT</sub> = 0.0V, $\overline{CS}$ = V <sub>IH2</sub>
I <sub>DD1</sub> <sup>[1]</sup>	Power Supply Current		35	50		40	60	mA	$\overline{CS}$ = V <sub>IH2</sub> , I <sub>OL</sub> = 0.0mA, T <sub>A</sub> = 25°C, Continuous
I <sub>DD2</sub>	Power Supply Current		32	46		37	55	mA	$\overline{CS}$ = 0.0V, I <sub>OL</sub> = 0.0mA, T <sub>A</sub> = 25°C, Continuous
I <sub>DD3</sub>	Power Supply Current		38	60		43	65	mA	$\overline{CS}$ = V <sub>IH2</sub> , I <sub>OL</sub> = 0.0mA, T <sub>A</sub> = 0°C, Continuous
I <sub>CF1</sub>	Output Clamp Current		8	14		7	13	mA	V <sub>OUT</sub> = -1.0V, T <sub>A</sub> = 0°C, Continuous
I <sub>CF2</sub>	Output Clamp Current		7	13		6	12	mA	V <sub>OUT</sub> = -1.0V, T <sub>A</sub> = 25°C, Continuous
I <sub>GG</sub>	Gate Supply Current			1			1	μA	
V <sub>IL1</sub>	Input Low Voltage for TTL Interface	-1		0.65	-1		0.65	V	
V <sub>IL2</sub>	Input Low Voltage for MOS Interface	V <sub>DD</sub>		V <sub>CC</sub> -6	V <sub>DD</sub>		V <sub>CC</sub> -6	V	
V <sub>IH1</sub>	Addr. Input High Voltage	V <sub>CC</sub> -2		V <sub>CC</sub> +0.3	V <sub>CC</sub> -2		V <sub>CC</sub> +0.3	V	
V <sub>IH2</sub>	Chip Sel. Input High Volt.	V <sub>CC</sub> -2		V <sub>CC</sub> +0.3	V <sub>CC</sub> -1.5		V <sub>CC</sub> +0.3	V	
I <sub>OL</sub>	Output Sink Current	1.6	4		1.6	4		mA	V <sub>OUT</sub> = 0.45V
I <sub>OH</sub>	Output Source Current	-2.0			-2.0			mA	V <sub>OUT</sub> = 0.0V
V <sub>OL</sub>	Output Low Voltage		-3	0.45		-3	0.45	V	I <sub>OL</sub> = 1.6mA
V <sub>OH</sub>	Output High Voltage	3.5	4.5		3.5	4.5		V	I <sub>OH</sub> = -200μA

Note 1: Typical values are at nominal voltages and T<sub>A</sub> = 25°C.

### A.C. Characteristics

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{DD} = -9\text{V} \pm 5\%$ ,  $V_{GG} = -9\text{V} \pm 5\%$  unless otherwise noted

Symbol	Test	1702A Limits		1702A-2 Limits		1702A-6 Limits		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Freq.	Repetition Rate		1		1.6		0.66	MHz
$t_{OH}$	Previous Read Data Valid		0.1		0.1		0.1	$\mu\text{s}$
$t_{ACC}$	Address to Output Delay		1		0.65		1.5	$\mu\text{s}$
$t_{CS}$	Chip Select Delay		0.1		0.3		0.6	$\mu\text{s}$
$t_{CO}$	Output Delay From $\overline{\text{CS}}$		0.9		0.35		0.9	$\mu\text{s}$
$t_{OD}$	Output Deselect		0.3		0.3		0.3	$\mu\text{s}$

PROM/ROM

### Capacitance\* $T_A = 25^\circ\text{C}$

SYMBOL	TEST	TYPICAL	MAXIMUM	UNIT	CONDITIONS
$C_{IN}$	Input Capacitance	8	15	pF	$V_{IN} = V_{CC}$ $\overline{\text{CS}} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$
$C_{OUT}$	Output Capacitance	10	15	pF	

All unused pins are at A.C. ground

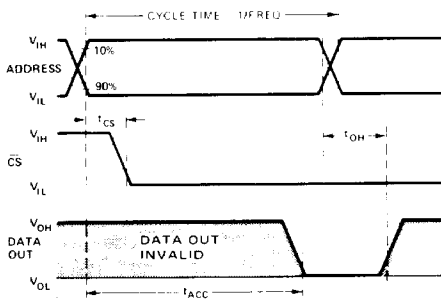
\*This parameter is periodically sampled and is not 100% tested.

### Switching Characteristics

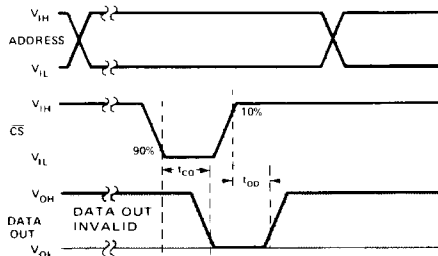
#### Conditions of Test:

Input pulse amplitudes: 0 to 4V;  $t_R, t_F \leq 50$  ns  
 Output load is 1 TTL gate; measurements made at output of TTL gate ( $t_{PD} \leq 15$  ns),  $C_L = 15$  pF

#### A) READ OPERATION



#### B) DESELECTION OF DATA OUTPUT IN OR-TIE OPERATION



# Typical Characteristics

PROM/ROM

